Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **IN1**
2. **D1**
3. **S1**
4. **V-**
5. **GND**
6. **S4**
7. **D4**
8. **IN4**
9. **IN3**
10. **D3**
11. **S3**
12. **VL**
13. **V+**
14. **S2**
15. **D2**
16. **IN2**

**.106”**

****

**.070”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004” min.**

**Backside Potential:**

**Mask Ref: CSHNC**

**APPROVED BY: DK DIE SIZE .070” X .106” DATE: 9/28/22**

**MFG: SILICONIX THICKNESS .000” P/N: DG411-DG413**

**DG 10.1.2**

#### Rev B, 7/19/02